REMARKS

Please reconsider the application in view of the above amendments and the following remarks. Applicants thank the Examiner for carefully considering this application.

Disposition of Claims

Claims 1-7 were pending in this application. By way of this reply, new claims 8-13 have been added. Thus, claims 1-13 are currently pending. Claims 1 and 8 are independent. The remaining claims depend directly from claims 1 and 8.

Claim Amendments

New claims 8-13 have been added by this reply. Support for new claims 8-13 may be found, for example, in the originally filed claims and in paragraphs [0026]-[0035] of the Published Specification. No new matter has been added by any of the new claims.

Rejection(s) under 35 U.S.C § 103

Claims 1, 3-7

Claims 1 and 3-7 stand rejected under 35 U.S.C. § 103 as being unpatentable over Admitted Prior Art ("APA") in view of U.S. Patent No. 6,068,192 ("McCabe"). For the reasons set forth below, the rejection is respectfully traversed.

One or more embodiments of the claimed invention are directed to a tamper proof chip card. For example, Figures 1 and 2 show a card body (10) and a chip module (12) including an integrated circuit ("IC"). In this embodiment, the card body (10) includes three layers (*i.e.*, a

security layer (26) disposed between a base layer (14) and an upper layer (16)). To protect against fraudulent use, the upper layer (16) may include one or more security features (*e.g.*, photograph of authorized user, laser engraving, holograms, etc.). In order to prevent tampering with the security features on the upper layer (16), the security layer (26) includes a conductive pattern (28) connected to the IC, such that the conductive pattern (28) forms an electric loop in security layer (26) with regions such as (30) and (32)that are located beneath security features of upper layer (16).

In this embodiment, the conductive pattern (28) acts as a switch that deactivates the IC (*i.e.*, deactivates use of the card) when the conductive pattern (28) is altered. More specifically, the conductive pattern (28) may include specific electrical properties (*e.g.*, a given impedance or resistance), such that the IC is adapted to compare the, *e.g.*, impedance, with a predetermined value stored in a memory of the IC. Thus, peeling off the upper layer (16) will alter electrical properties of the conductive pattern such that the conductive pattern no longer matches the predetermined value stored within the IC, thereby deactivating the chip card. *See* Published Specification, pars. [0026]-[0035].

Turning to the rejection, independent claim 1 recites, *inter alia*,

> wherein said card body comprises an additional tamper-detection layer including a conductive pattern forming an electrical loop connected between terminals of the integrated circuit, said conductive pattern having at least one region located beneath or above said security feature, and wherein said integrated circuit is adapted to perform an integrity check of said conductive pattern for conditionally performing further operations only in case said integrity is recognized.

The aforementioned limitations require: (i) a tamper-detection layer *including an electrical loop*, such that the *tamper-detection layer is an additional distinct layer* to the card body; (ii) a *conductive pattern* having at least one *region located beneath or above the security feature*; and (iii) an

integrated circuit adapted to *perform an integrity check*. *See e.g.*, Published Specification, pars. [0026]-[0035].

In order to establish a *prima facie* case of obviousness, the cited references must teach or suggest all the limitations of the claims. *See* MPEP § 2143. The Examiner admits that APA fails to disclose "an additional tamper-detection layer including a conductive pattern forming an electrical loop connected between terminals of IC." *See* Office Action mailed July 26, 2007, p. 3. Rather, the Examiner relies on McCabe to teach that which APA lacks. The Applicants respectfully assert that McCabe fails to teach or suggest that which APA lacks.

McCabe fails to teach or suggest an additional tamper detection layer including an electrical loop

Rather, McCabe is directed only to protecting against a single type of unauthorized tampering (*i.e.*, the unauthorized separation of the first housing portion from the second housing portion) of a smart card body. *See* McCabe, col. 5, ll. 17-37. On page 3 of the Action, the Examiner cites McCabe as teaching "a smart card having a tamper detection layer with a conductive pattern" and fails to cite any reference as disclosing, teaching, or suggesting an *additional* tamper detection layer *including* a conductive pattern forming *an electrical loop*. The Examiner's failure to cite a single reference as showing the aforementioned limitations effectively acknowledges that neither of the cited references teach an additional tamper detection layer having an electrical loop.

Further, the cited portion of McCabe (col. 5, ll. 35-37), which is associated with Figure 1, clearly depicts only a first and a second housing portion (*i.e.*, fails to teach or suggest an additional tamper-resistant layer). Moreover, Applicants respectfully assert that McCabe is silent with respect to a single layer (*i.e.*, tamper-resistant layer) which houses a conductive pattern

forming an electrical loop. Rather, McCabe shows a first housing portion and a second housing portion, each including a portion of a conductor (in contrast to a conductive pattern housed by a single layer). Assuming *arguendo* that the Examiner equates the conductor of McCabe with the conductive pattern of the claimed invention, Applicants respectfully assert that the conductor of McCabe fails to form *an electric loop on a single layer*. Rather, the two conductors (each on a separate housing portion) are only joined together once the first housing portion and second housing portion are joined together. Thus, McCabe is silent with respect to an additional tamper resistant layer, such that the tamper-resistant layer comprises the conductive pattern forming an electric loop as required by independent claim 1.

McCabe fails to teach or suggest a conductive pattern located beneath or above security features

Further, McCabe is silent with respect to a conductive pattern having at least one region located beneath or above security features as required by the claimed invention. This is evidenced by the fact that the Examiner fails to cite any reference as disclosing, teaching, or suggesting the above limitation, thereby acknowledging that neither of the cited references teach a conductive pattern located beneath or above security features.

Moreover, as shown in Figure 1 of McCabe, two separate conductors are connected together by joining the first housing portion to the second housing portion, thereby forming a rectangle concentrated toward the center of the smart card body. McCabe is silent with respect to a conductive pattern beneath or above security features. In fact, McCabe is specifically directed toward protecting the card body from an unauthorized separation of the first and second housing portions (causing an interruption in electric flow). *See* McCabe, col. 5, ll. 17-37. Thus, McCabe is

silent with respect to a conductive pattern having at least one region located beneath or above said security features as required by independent claim 1.

McCabe fails to teach or suggest an IC adapted to perform an integrity check

Further still, McCabe is silent with respect to an IC adapted to perform an integrity check of the conductive pattern for conditionally performing further operations only in case the integrity is recognized. This is evidenced by the fact that the Examiner fails to cite any reference as disclosing, teaching, or suggesting the above limitation, thereby acknowledging that neither of the cited references teach an integrated circuit adapted to perform an integrity check. To that end, as discussed previously, McCabe's conductor circuit is only alerted to tampering when the housing separations are separated. McCabe never discloses an IC able to perform an integrity check (*e.g.*, comparison of impedance or resistance of the circuit with a predetermined value) *on a separate electrical loop* for conditionally performing further operations only in case the integrity is recognized.

Because McCabe fails to teach or suggest the aforementioned limitations, the Examiner has failed to establish a *prima facie* case of obviousness using APA and McCabe. Accordingly, independent claim 1 is patentable over APA and McCabe. Dependent claims are patentable for at least the same reasons as claim 1. Accordingly, withdrawal of this rejection is respectfully requested.

Claim 2

Claim 2 stands rejected under 35 U.S.C. § 103 as being unpatentable over APA in view of McCabe, and further in view of U.S. Patent No. 6,491,215 ("Irwin"). To the extent that this rejection applies to claim 1, the rejection is respectfully traversed.

Claim 2 depends from independent claim 1. As discussed previously, APA and McCabe, whether considered separately or in combination, fail to teach or suggest all the limitations of independent claim 1. Further, Irwin fails to teach or suggest that which APA and McCabe lack as evidenced by the fact that Irwin is only relied upon to teach "a conductive pattern having a given impedance and the IC is adapted to check the resistance matches a predetermined value stored in a memory," *See* Office Action mailed July 26, 2007, p. 5. In view of the above, the Examiner has failed to establish a *prima facie* case of obviousness using APA, McCabe, and Irwin. Accordingly, independent claim 1 and dependent claim 2 are patentable over APA, McCabe, and Irwin. Withdrawal of this rejection is respectfully requested.

New Claims

Claims 8-13 have been added by this reply. Support for new claims 8-13 may be found, for example, in paragraphs [0026]-[0035] of the Published Specification.

With respect to new independent claim 8, new independent claim 8 includes essentially the same patentable limitations as independent claim 1 and, thus, is patentable over the cited references for at least the same reason as independent claim 1. New dependent claims are patentable over the cited references for at least the same reason as independent claim 1 and new independent claim 8.

In addition, new independent claim 8 recites, in part,

> A chip card comprising:
> a base layer;
> an upper layer comprising an integrated circuit, wherein at least one security feature is located on the upper layer; and
> a security layer interposed between the base layer and the upper layer, …

The Applicants respectfully assert that none of the cited references teach or suggest the aforementioned limitations. Specifically, McCabe only discloses a first housing portion and a second housing portion, and is silent with respect to a third layer (*i.e.*, security layer). *See e.g.*, McCabe, Figure 1. Further, APA and Irwin are also silent with respect to a third layer (*i.e.*, security layer). Thus, APA, McCabe, and Irwin, whether considered separately or in combination, fail to teach or suggest the above limitation.

In view of the above, new claims 8-13 are patentable over the cited prior art references. Accordingly, favorable action in the form of a Notice of Allowability is respectfully requested.

Conclusion

Applicants believe this reply is fully responsive to all outstanding issues and places this application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 09669/080001).

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Respectfully submitted,

By _____

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